WHAT IS CLAIMED IS:

1. A clock multiplying PLL circuit, comprising:

an oscillator circuit for outputting an output clock signal;

first through n-th dividers for dividing the output clock signal and thereby outputting first through n-th divided signals (where n: an integer greater than or equal to 2) respectively, said first through n-th dividers being different in effective transition timings of the outputted first through n-th divided signals from one another;

a reference clock signal generating circuit for generating n types of first through n-th reference clock signals different in phase from one another by using an input reference clock signal; and

first through n-th phase comparators for respectively comparing phases of the i-th reference clock signals and i-th divided signals (where i: an integer of 1 to n),

wherein an oscillation frequency of the output clock signal outputted from the oscillator circuit is changed based on the results of comparisons by the first through n-th phase comparators.

2. A clock multiplying PLL circuit according to claim 1, wherein the first through n-th dividers respectively have the same dividing ratio 1/M (where M: an integer greater than or equal to 2), and

when the number of pulses of the output clock signal outputted from the oscillator circuit is taken as Pj during a period from the effective transition timing of the first divided signal to the effective transition timing of the j-th divided

signal (where j: an integer of 2 to n), a phase delay of a j-th reference clock signal when the first reference clock signal is set as the reference, is Pj/M cycles.

3. A clock multiplying PLL circuit according to claim 2, further including divider initial reset means for resetting the first divider once alone with an effective transition timing of the first reference clock signal generated from the reference clock signal generating circuit in wait for the start of the output of the output clock signal from the oscillator circuit after powering the clock multiplying PLL circuit, and resetting the j-th dividers corresponding to the remaining second through n-th dividers once alone, respectively, with timing at which the number of pulses of the output clock signal outputted from the oscillator circuit after the resetting of the first divider reaches the Pj.

4. The clock multiplying PLL circuit according to claim 1, wherein the first through n-th dividers respectively have the same dividing ratio 1/M (where M: an integer greater than or equal to 2),

the number of pulses of an output clock signal outputted from the oscillator circuit is set as M·(j-1)/n during a period from the effective transition timing of the first divided signal to an effective transition timing of a j-th divided signal (where j: an integer of 2 to n), and

a phase delay of a j-th reference clock signal when the first reference clock signal is set as the reference, is (j-1)/n cycles.

5. A clock multiplying PLL circuit according to claim 4, further including divider initial reset means for resetting the first divider once alone with an effective transition timing of the first reference clock signal generated from the reference clock signal generating circuit in wait for the start of the output of the output clock signal from the oscillator circuit after powering the clock multiplying PLL circuit, and resetting the j-th dividers corresponding to the remaining second through n-th dividers once alone, respectively, with timing at which the number of pulses of the output clock signal outputted from the oscillator circuit after the resetting of the first divider reaches the $M\cdot(j-1)/n$.

6. A clock multiplying PLL circuit according to claim 5, wherein the divider initial reset means includes a reset divider of a dividing ratio 1/(M/n) reset together with the first divider with the effective transition timing of the first reference clock signal, and

sequential reset means for sequentially resetting the second through n-th dividers in accordance with a divided signal of the reset divider.

7. A clock multiplying PLL circuit according to claim 1, wherein the oscillator circuit is a voltage-controlled oscillator, and which further includes,

an up signal adder for adding first through n-th up signals of respective results of comparisons by the first through n-th phase comparators,

a down signal adder for adding first through n-th down signals thereof,

a charge pump for inputting the added up signal and the added down signal, and

a low-pass filter for smoothing a signal outputted from the charge pump and inputting the smoothed output to the voltage-controlled oscillator.

8. A clock multiplying PLL circuit according to claim 2, wherein the oscillator circuit is a voltage-controlled oscillator, and which further includes,

an up signal adder for adding first through n-th up signals of respective results of comparisons by the first through n-th phase comparators,

a down signal adder for adding first through n-th down signals thereof,

a charge pump for inputting the added up signal and the added down signal, and

a low-pass filter for smoothing a signal outputted from the charge pump and inputting the smoothed output to the voltage-controlled oscillator.

9. A clock multiplying PLL circuit according to claim 3, wherein the oscillator circuit is a voltage-controlled oscillator, and which further includes,

an up signal adder for adding first through n-th up signals of respective results of comparisons by the first through n-th phase comparators,

a down signal adder for adding first through n-th down signals thereof,

a charge pump for inputting the added up signal and the added down signal, and

a low-pass filter for smoothing a signal outputted from the charge pump and inputting the smoothed output to the voltage-controlled oscillator.

10. A clock multiplying PLL circuit according to claim 4, wherein the oscillator circuit is a voltage-controlled oscillator, and which further includes,

an up signal adder for adding first through n-th up signals of respective results of comparisons by the first through n-th phase comparators,

a down signal adder for adding first through n-th down signals thereof,

a charge pump for inputting the added up signal and the added down signal, and

a low-pass filter for smoothing a signal outputted from the charge pump and inputting the smoothed output to the voltage-controlled oscillator.

11. A clock multiplying PLL circuit according to claim 5, wherein the oscillator circuit is a voltage-controlled oscillator, and which further includes,

an up signal adder for adding first through n-th up signals of respective results of comparisons by the first through n-th phase comparators,

a down signal adder for adding first through n-th down signals thereof,

a charge pump for inputting the added up signal and the added down signal, and

a low-pass filter for smoothing a signal outputted from the charge pump and inputting the smoothed output to the

voltage-controlled oscillator.

12. A clock multiplying PLL circuit according to claim 6, wherein the oscillator circuit is a voltage-controlled oscillator, and which further includes,

an up signal adder for adding first through n-th up signals of respective results of comparisons by the first through n-th phase comparators,

a down signal adder for adding first through n-th down signals thereof,

a charge pump for inputting the added up signal and the added down signal, and

a low-pass filter for smoothing a signal outputted from the charge pump and inputting the smoothed output to the voltage-controlled oscillator.

13. A clock multiplying PLL circuit according to claim 1, wherein the reference clock signal generating circuit is a delay locked loop circuit for delaying the reference clock signal and thereby generating the first through n-th reference clock signals.

14. A clock multiplying PLL circuit according to claim 2, wherein the reference clock signal generating circuit is a delay locked loop circuit for delaying the reference clock signal and thereby generating the first through n-th reference clock signals.

15. A clock multiplying PLL circuit according to claim 3, wherein the reference clock signal generating circuit is a delay

locked loop circuit for delaying the reference clock signal and thereby generating the first through n-th reference clock signals.

16. A clock multiplying PLL circuit according to claim 4, wherein the reference clock signal generating circuit is a delay locked loop circuit for delaying the reference clock signal and thereby generating the first through n-th reference clock signals.

17. A clock multiplying PLL circuit according to claim 5, wherein the reference clock signal generating circuit is a delay locked loop circuit for delaying the reference clock signal and thereby generating the first through n-th reference clock signals.

18. A clock multiplying PLL circuit according to claim 6, wherein the reference clock signal generating circuit is a delay locked loop circuit for delaying the reference clock signal and thereby generating the first through n-th reference clock signals.

19. A clock multiplying PLL circuit for PLL-controlling an oscillator circuit and outputting an output clock signal having multiplied frequency obtained by multiplying an input reference clock signal, comprising:

n (where n: an integer greater than or equal to 2) dividers having the same dividing ratio and for dividing the output clock signal;

n-pieces of phase comparators paired with the dividers; and

a reference clock signal generating circuit for generating n types of reference clock signals different in phase from one another using the reference clock signal,

wherein each of the phase comparators obtains a result of phase comparison from a phase comparison between each of divided signals outputted from the dividers paired with the phase comparators and any of the n types of reference clock signals, and the oscillator circuit is PLL-controlled by n times for each cycle period of the reference clock signal by use of the result of phase comparison.

20. A clock multiplying PLL circuit for outputting an output clock signal having multiplied frequency obtained by multiplying an input reference clock signal, comprising:

an oscillator circuit; and

a multiple control circuit for performing PLL-control on the oscillator circuit by a predetermined number of times greater than or equal to 2 for each cycle period of the reference clock signal.